

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 47 (Cancelled).

48. (New) A method for on demand functional verification of a software model of an application specific integrated circuit (ASIC), wherein said software model is written in a low-level programming language and the method separately establishes a model of the application specific integrated circuit to be generated and functional verification tests to be applied to the model of the circuit for constituting a verification platform comprising a transmission mode and a verification mode, the method comprising:

creating, in the transmission mode, an autonomous circuit emulator constituted with a data processing system, obtained by replacing the software model which is in a low level programming language and that physically describes an ASIC comprising a circuit under design to be validated, with a high level language abstract description generating response data structures in accordance with a functional specification of the project as a function of stimuli received;

integrating the software model, in a verification mode, into a verification platform, and connecting a previously validated autonomous circuit emulator in parallel to interfaces of the software model of the circuit under design, and to an environment emulator;

utilizing the verification platform as a reference for the validation of response data transmitted by the software model of the circuit under design; and

outputting one or more error notifications if an error is detected by said validation.

49. (New) A method according to claim 48, further comprising:

generating, using a data processing system and in response to a user input, the autonomous circuit emulator which provides a simulation configuration corresponding to the software model of the ASIC using the functional specification;

writing, from the functional specification, and storing in a test platform for integrated circuit models, a program for testing the software model of the ASIC, comprising input stimuli sequences to be provided to the software model of the ASIC, related to output stimuli sequences by the autonomous simulation configuration, based on the functional specification;

linking together, and activating, the autonomous simulation configuration and the test platform; and

observing the output stimuli of the software model of the ASIC, wherein the software model of the ASIC is a Hardware Description Language (HDL)-type model, in order to functionally validate the system constituted by the software model of the ASIC and a validation test program, and thus validating the software model in comparison to the functional specification.

50. (New) A method according to claim 48, wherein the autonomous configuration communicates with the user to control the activation of previously created and stored models of input stimuli sequences defined in a high-level programming language, and controls the activation of associated programs for the progressive validation of test sequences determined from the models.

51. (New) A method according to claim 48, wherein the functional specification comprises a sequence of instructions in a low-level programming language, specifying functional models of circuits.

52. (New) A method according to claim 48, wherein the functional specification is provided in the form of a first specification program in a low level programming language of functional models of circuits, and a second specification program in a high level programming language of functional models of circuits, and the autonomous simulation configuration performs a co-simulation by synchronizing the execution of the first and second specification programs.

53. (New) A method according to claim 52, wherein the low level language is a Hardware Description Language (HDL)-type and the high level language is C++.

54. (New) A method according to claim 48, wherein the verification platform verifies that the responses of the software model of the ASIC are within response time ranges specified in the functional specification.

55. (New) A verification platform for on demand verification of a software model of an application specific integrated circuit (ASIC), comprising data processing means for allowing a client to select test models producing input stimuli for the ASIC, said data processing means being constructed and arranged to read functional specification elements of the ASIC in a high level language and comprising a sequence of programmed instructions that form an emulator and generate a functional validation test program constituted by output stimuli, from the input stimuli and the functional specification elements, and that output one or more error notifications if an error is detected by said functional validation test program.

56. (New) A verification platform according to claim 55, further comprising a library of functional models of circuit blocks for a plurality of ASICs and means for selecting models through a definition file of the integrated circuit configuration, for creating a model corresponding to the functional specification of one of said plurality of ASICs that is integrated into the definition of an environment of the ASIC.

57. (New) A verification platform according to claim 55, further including, in a link connecting the platform to a client, first and second serial programming language adaptation circuits, wherein the first serial programming language adaptation circuit transforms commands in a high level programming language used by the client into commands in a low level programming language used by the ASIC model, and wherein the second serial programming language adaptation circuit transforms the commands in the low level programming language back into commands in the high level programming language.

58. (New) A verification platform according to claim 55, further comprising means for executing operations at the same time as the simulation, and, upon detection of an error, means for interrupting operations at the time the error appears.

59. (New) A verification platform according to claim 55, wherein the functional specification elements are constituted by a truth table corresponding to the functions of the various functional circuit elements of the ASIC software model, and further comprising a propagation delay associated with each input and each output pair.

60. (New) A verification platform according to claim 55, wherein the functional specification elements are constituted by a behavior table corresponding to the functions of the various functional circuit elements of the ASIC software model, and further comprising a propagation delay associated with each input and each output pair.

61. (New) A verification platform according to claim 55, further including a cache memory for storing the blocks used by nodes according to node addresses, and means for managing, for an address used by one or more nodes, a presence vector with one presence indicator per node.

62. (New) A verification platform according to claim 61, wherein the programmed instructions are object-oriented and the emulator is structured as a set of classes for managing a collection of execution hypotheses for a transaction in a memory block of the software model, and for managing transactions that are concurrently colliding using the same memory block.

63. (New) A verification platform according to claim 61, wherein algorithms of the sequence of programmed instructions of the emulator are configured to cause the emulator to perform functions comprising generating predictions, eliminating predictions, readjusting incorrect predictions, reducing the number of valid hypotheses, and terminating collisions.

64. (New) A verification platform according to claim 63, wherein the emulator of the ASIC circuit generates predictions without having to obtain additional information on the internal operation of the ASIC circuit, the ASIC circuit being a circuit under design.

65. (New) A verification platform according to claim 61, wherein the platform is used as an emulator of a router circuit, a circuit with cache or a router circuit with cache.

66. (New) A verification platform according to claim 61, wherein the platform is configured for testing a software model of an integrated circuit (ASIC) on demand and comprises an ASIC emulator for controlling a comparator that receives values generated by a software model of the ASIC circuit tested, upon reception of stimuli sent by at least one stimuli generating circuit storing a test program, an interface for translating the stimuli from an advanced language into a low level language corresponding to that of the software model, and means for validating the verification in case of the detection of a collision by the comparator.

67. (New) A verification platform according to claim 61, further comprising means for selecting the response to stimuli that depend on the composition of the circuits tested, said means for selecting being constituted by a model generated by means for selecting functional models from a library, which associates with each of the models the responses to a given stimulus, the model corresponding to the composition of the circuit to be tested.

68. (New) A verification platform according to claim 67, further including means for storing responses selected so as to create a test model to be applied to the circuit tested during the reception of stimuli.

69. (New) A verification platform according to claim 55, wherein each transaction comprises, at the level of each interface, a request packet and one or more associated response packets, wherein the values of the parameters and/or the transmission time constraints of the request packet and one or more associated response packets can be forced from the functional test program executed by the emulator of the environment, which appropriately translates all of said parameters during the transmission of the request packet and one or more associated response packets to the terminals of the software model of the design.

70. (New) A verification platform according to claim 68, wherein the generation of predictions is performed by the emulator of the circuit without having to obtain additional information on the internal operation of the circuit, the circuit being a circuit under design.

71. (New) A computer-readable medium upon which is embodied a sequence of programmed instructions that, when executed by a processor, cause the processor to perform a method for on demand functional verification of a software model of an application specific integrated circuit (ASIC), wherein said software model is written in a low-level programming language and the method separately establishes a model of the application specific integrated circuit to be generated and functional verification tests to be applied to the model of the circuit for constituting a verification platform comprising a transmission mode and a verification mode, the method comprising:

creating, in the transmission mode, an autonomous circuit emulator constituted with a data processing system, obtained by replacing the software model which is in a low level programming language and that physically describes an ASIC comprising a circuit under design to be validated, with a high level language abstract description generating response data structures in accordance with a functional specification of the project as a function of stimuli received;

integrating the software model, in a verification mode, into a verification platform, and connecting a previously validated autonomous circuit emulator in parallel to interfaces of the software model of the circuit under design, and to an environment emulator;

utilizing the verification platform as a reference for the validation of response data transmitted by the software model of the circuit under design; and

outputting one or more error notifications if an error is detected by said validation.

72. (New) A computer readable medium according to claim 71, further comprising programmed instructions for:

generating, using a data processing system and in response to a user input, the autonomous circuit emulator which provides a simulation configuration corresponding to the software model of the ASIC using the functional specification;

writing, from the functional specification, and storing in a test platform for integrated circuit models, a program for testing the software model of the ASIC, comprising input stimuli sequences to be provided to the software model of the ASIC, related to output stimuli sequences by the autonomous simulation configuration, based on the functional specification;

linking together, and activating, the autonomous simulation configuration and the test platform; and

observing the output stimuli of the software model of the ASIC, wherein the software model of the ASIC is a Hardware Description Language (HDL)-type model, in order to functionally validate the system constituted by the software model of the ASIC and a validation test program, and thus validating the software model in comparison to the functional specification.